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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,671	03/18/2004	Katsuhiro Watanabe	7651-US0	8002

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,671	WATANABE ET AL.	
	Examiner	Art Unit	
	JASON M. PERILLA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending in the instant application.

Response to Argument

2. The Applicant's argument, filed November 13, 2007, has been fully considered, but it is not persuasive.

The Applicant states that "Jungerman does not indicate how the external clock is recovered from the repetitive pattern, . . . and no phase locked loop circuit is shown in Jungerman." However, as broadly as claimed, Jungerman's "recovered" clock is the sampled version of the repetitive pattern external data (fig. 1B, ref. 11; col. 2, lines 41-42; col. 2, lines 49-53). It is "recovered" as it is sampled. Moreover, Jungerman (or the combination of Jungerman in view of Soma) does not need to disclose a phase locked loop circuit. Rather, only the "simulation" of a phase locked loop circuit is claimed. Indeed, the Applicant's representative figures of the claimed invention (i.e. figs. 3 and 4) *do not contain a phase locked loop*. The use of a phase locked loop is rendered unnecessary by the Applicant's claimed embodiment of the invention. The combination of Jungerman in view of Soma "simulates" a phase locked loop for at least the same reasons as those of the instant invention because they each perform the same method steps. In the combination of Jungerman in view of Soma, Jungerman's repetitive pattern external data (fig. 1B, ref. 11) is replaced by a clock signal as suggested by Soma. It is this clock signal which is later "recovered" when it is sampled.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jungerman et al (U.S. Pat. No. 7206340; "Jungerman") in view of Soma et al (U.S. Pat. No. 6775321; "Soma").

Regarding claim 1, Jungerman discloses a method in an apparatus that receives external clock (fig. 1B, ref. 15) and "repetitive pattern" external data (fig. 1B, ref. 11) signals for recovering a pattern from said external data, comprising the steps of: digitizing (col. 2, lines 41-42; col. 2, lines 49-53) said external data signal to obtain time domain data and storing said time domain data in a memory (inherent); detecting time domain data of edges (col. 2, lines 40-50; fig. 2, ref. 22) of said external data signal; and, converting said detected time domain data of said edges of into frequency domain data (fig. 2, ref. 28; col. 3, lines 10-20). Jungerman discloses a method of analyzing jitter in a periodic or "repetitive" signal (col. 1, lines 10-20; col. 1, lines 35-60). The

periodic signal is sampled, stored, edge detected, and converted into the frequency domain. In the frequency domain, identified peaks of the signal are truncated (fig. 2, ref. 30). An RMS value corresponding to the truncated signal's spectrum is determined (fig. 3, ref. 32), and it is utilized, after a frequency to time conversion (fig. 2, ref. 40), to determine jitter in the periodic signal (fig. 2, ref. 40). Jungerman discloses that a "repetitive pattern" signal is analyzed rather than a clock signal. Further, Jungerman does not explicitly disclose multiplying said frequency domain data by respective predetermined coefficients in different frequency domains. However, Soma teaches, in a strictly analogous jitter determination method (col. 1, lines 5-7), analyzing a clock signal (fig. 1, output of PLL 11) by sampling (fig. 4, ref. 15) the signal, performing a time to frequency domain transformation upon the samples (fig. 43, ref. 1501), applying a bandwidth filter against the frequency domain representation of the signal's samples (fig. 43, ref. 1502), and performing a frequency to time domain transformation upon the filtered frequency domain representation of the signal's samples (fig. 43, ref. 1503). The implementation of the bandwidth filter is described by Soma in column 13, lines 35-55. Soma describes that the digitized (i.e. sampled) 400Mhz clock's frequency domain representation is augmented such that only the "data around the fundamental frequency 400Mhz in the positive frequency components of the spectrum X(f) are retained, and the remaining data made zero." Furthermore, Soma describes that "the positive frequency components are doubled" or, stated alternatively, multiplying said frequency domain data by respective predetermined coefficients (doubling; x2) in different frequency domains (i.e. "the positive frequency components of the spectrum X(f)"). According to

the treachings of Soma, one skilled in the art would have recognized that Soma's frequency domain coefficient multiplying has the effect of reducing spurious frequencies in the received clock signal such that a reference clock signal is created to permit a jitter measurement against the original received clock signal. Furthermore, it has been held that one skilled in the art of electronics has a high level of skill generally holding a bachelors or masters degree in electrical engineering. See *Medtronic, Inc. v. Cardiac Pacemakers, Inc.*, 555 F.Supp. 1214, 1221 (D.C. Minn. 1983). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that Jungerman's jitter measurement method could be applied to a clock signal and that the frequency domain representation of the samples of the clock signal could be multiplied by predetermined coefficients as taught by Soma because it would permit the creation of a reference clock signal without spurious frequency components for the determination of jitter.

Regarding claim 2, Jungerman in view of Soma disclose the limitations of claim 1 as applied above. Jungerman in view of Soma do not explicitly disclose that the coefficients are selected to simulate a filter corresponding to said phase lock loop (PLL) circuit. However, the coefficients do simulate a PLL circuit because they remove spurious frequencies in the received clock signal. One skilled in the art is aware that a PLL acts as a "filter" for a received clock signal. Effectively, the frequency domain coefficients act as a filter just as a PLL does.

Regarding claim 3, Jungerman in view of Soma disclose the limitations of the claim as applied to claim 1 above. Further, in the combination of Jungerman in view of

Soma, the digital samples of the received clock signal, after filtering in the time domain, are compared with the original received clock signal to make a determination of jitter.

Regarding claim 4, Jungerman in view of Soma disclose the limitations of claim 3 as applied above. Further, Jungerman in view of Soma disclose the remaining limitations of the claim as applied to claim 2 above.

Regarding claim 5, Jungerman in view of Soma disclose the limitations of the claim as applied to claim 3 above.

Regarding claim 6, Jungerman in view of Soma disclose the limitations of claim 5 as applied above. Further, Jungerman in view of Soma disclose the remaining limitations of the claim as applied to claim 2 above.

Regarding claim 7, Jungerman in view of Soma disclose the limitations of the claim as applied to claim 1 above.

Regarding claim 8, Jungerman in view of Soma disclose the limitations of claim 7 as applied above. Further, Jungerman in view of Soma disclose the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 9, Jungerman in view of Soma disclose the limitations of claim 7 as applied above. Further, it is inherent in the method of Jungerman in view of Soma that the digitized received clock and frequency to time converted (and filtered) clock must be stored in a memory. Further, these groups of data are compared to determine jitter between the original clock signal and the filtered reference clock signal (Jungerman; fig. 2, ref. 40).

Regarding claim 10, Jungerman in view of Soma disclose the limitations of claim 7 as applied above. Further, Jungerman in view of Soma disclose the remaining limitations of the claim as applied to claim 2 above.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M. Perilla/
July 22, 2008

/jmp/

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611